Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the applications:

Listing of Claims:

1. (Original) A method for comparing integrated circuit technologies, comprising:

(a) receiving input variables for a plurality of integrated circuit technologies;

(b) processing said common input variables; and

(c) displaying at least one output variable for each of said plurality of integrated circuit technologies in a graphical form so that said plurality of integrated circuit technologies are comparable based on said at least one output variable.

2. (Currently Amended) The method of claim 1, wherein said plurality of integrated circuit technologies comprises ~~RapidChip™~~ Platform ASIC (application-specific integrated circuit).

3. (Original) The method of claim 2, wherein said plurality of integrated circuit technologies further comprises ASIC (application-specific integrated circuit) and FPGA (field-programmable gate array).

4. (Original) The method of claim 1, wherein said input variables comprise number of customizable gates, maximum time to prototype, and yearly product volume.

5. (Original) The method of claim 4, wherein said input variables further comprise number of IP (intellectual property) blocks.

6. (Original) The method of claim 1, wherein said input variables are set with sliders

in a task window of a graphical user interface by a user.

7. (Original) The method of claim 1, wherein said at least one output variable comprises risk and cost.

8. (Original) The method of claim 7, wherein said graphical form is a 3-D plot having a first axis for time to prototype, a second axis for said cost, and a third axis for said risk.

9. (Original) The method of 8, wherein each of said plurality of integrated circuit technologies has a separate 3-D plot.

10. (Original) The method of claim 1, wherein said at least one output variable comprises success and cost.

11. (Original) The method of claim 10, wherein said graphical form is a 3-D plot having a first axis for time to prototype, a second axis for said cost, and a third axis for said success.

12. (Original) The method of 11, wherein said plurality of integrated circuit technologies have a single 3-D plot, and each of said plurality of integrated circuit technologies is represented by different color.

13. (Original) The method of claim 1, wherein said graphical form comprises a scatter plot having a first axis for time to prototype, a second axis for number of customizable gates, and a third axis for yearly volume, said scatter plot having a plurality of dots, each dot in color representing one of said plurality of integrated circuit technologies with the least cost or in color representing infeasibility.

14. (Original) The method of claim 13, wherein said graphical form further comprises a bar chart showing a slack profit for one of said plurality of integrated circuit

technologies for a selected dot.

15. (Original) The method of claim 14, wherein when a user moves a value along one of said axes of said scatter plot, said bar chart changes dynamically in real time.

16. (Original) A computer-readable medium having computer-executable instructions for performing a method for comparing integrated circuit technologies, said method comprising steps of:

(a) receiving input variables for a plurality of integrated circuit technologies;

(b) processing said common input variables; and

(c) displaying at least one output variable for each of said plurality of integrated circuit technologies in a graphical form so that said plurality of integrated circuit technologies are comparable based on said at least one output variable.

17. (Currently Amended) The computer-readable medium of claim 16, wherein said plurality of integrated circuit technologies comprises ~~RapidChip~~™ Platform ASIC (application-specific integrated circuit).

18. (Original) The computer-readable medium of claim 17, wherein said plurality of integrated circuit technologies further comprises ASIC (application-specific integrated circuit) and FPGA (field-programmable gate array).

19. (Original) The computer-readable medium of claim 16, wherein said input variables comprise number of customizable gates, maximum time to prototype, and yearly product volume.

20. (Original) The computer-readable medium of claim 19, wherein said input variables further comprise number of IP (intellectual property) blocks.

21. (Original) The computer-readable medium of claim 16, wherein said input variables are set with sliders in a task window of a graphical user interface by a user.

22. (Original) The computer-readable medium of claim 16, wherein said at least one output variable comprises risk and cost.

23. (Original) The computer-readable medium of claim 22, wherein said graphical form is a 3-D plot having a first axis for time to prototype, a second axis for said cost, and a third axis for said risk.

24. (Original) The computer-readable medium of 23, wherein each of said plurality of integrated circuit technologies has a separate 3-D plot.

25. (Original) The computer-readable medium of claim 16, wherein said at least one output variable comprises success and cost.

26. (Original) The computer-readable medium of claim 25, wherein said graphical form is a 3-D plot having a first axis for time to prototype, a second axis for said cost, and a third axis for said success.

27. (Original) The computer-readable medium of 26, wherein said plurality of integrated circuit technologies have a single 3-D plot, and each of said plurality of integrated circuit technologies is represented by different color.

28. (Original) The computer-readable medium of claim 16, wherein said graphical form comprises a scatter plot having a first axis for time to prototype, a second axis for number of customizable gates, and a third axis for yearly volume, said scatter plot having a plurality of dots, each dot in color representing one of said plurality of integrated circuit technologies with the least cost or in color representing infeasibility.

29. (Original) The computer-readable medium of claim 28, wherein said graphical form further comprises a bar chart showing a slack profit for one of said plurality of integrated circuit technologies for a selected dot.

30. (Original) The computer-readable medium of claim 29, wherein when a user moves a value along one of said axes of said scatter plot, said bar chart changes dynamically in real time.

31. (Original) A computer system comprising:

a central processing unit;

a display operatively coupled to said central processing unit; and

memory operatively coupled to said central processing unit, said memory including an operating system having a graphical user interface;

wherein via said graphical user interface, said computer system receives input variables for a plurality of integrated circuit technologies, and, after processing said common input variables, displaying at least one output variable for each of said plurality of integrated circuit technologies in a graphical form so that said plurality of integrated circuit technologies are comparable based on said at least one output variable.

32. (Currently Amended) The computer system of claim 31, wherein said plurality of integrated circuit technologies comprises ~~RapidChip~~™ Platform ASIC (application-specific integrated circuit).

33. (Original) The computer system of claim 32, wherein said plurality of integrated circuit technologies further comprises ASIC (application-specific integrated circuit) and FPGA (field-programmable gate array).

34. (Original) The computer system of claim 31, wherein said input variables comprise number of customizable gates, maximum time to prototype, and yearly product volume.

35. (Original) The computer system of claim 34, wherein said input variables further comprise number of IP (intellectual property) blocks.

36. (Original) The computer system of claim 31, wherein said input variables are set with sliders in a task window of said graphical user interface by a user.

37. (Original) The computer system of claim 31, wherein said at least one output variable comprises risk and cost.

38. (Original) The computer system of claim 37, wherein said graphical form is a 3-D plot having a first axis for time to prototype, a second axis for said cost, and a third axis for said risk.

39. (Original) The computer system of 38, wherein each of said plurality of integrated circuit technologies has a separate 3-D plot.

40. (Original) The computer system of claim 31, wherein said at least one output variable comprises success and cost.

41. (Original) The computer system of claim 40, wherein said graphical form is a 3-D plot having a first axis for time to prototype, a second axis for said cost, and a third axis for said success.

42. (Original) The computer system of 41, wherein said plurality of integrated circuit technologies have a single 3-D plot, and each of said plurality of integrated circuit technologies is represented by different color.

43. (Original) The computer system of claim 31, wherein said graphical form comprises a scatter plot having a first axis for time to prototype, a second axis for number of customizable gates, and a third axis for yearly volume, said scatter plot having a plurality of dots, each dot in color representing one of said plurality of integrated circuit technologies with the least cost or in color representing infeasibility.

44. (Original) The computer system of claim 43, wherein said graphical form further comprises a bar chart showing a slack profit for one of said plurality of integrated circuit technologies for a selected dot.

45. (Original) The computer system of claim 44, wherein when a user moves a value along one of said axes of said scatter plot, said bar chart changes dynamically in real

time.

46. (Original) The computer system of claim 31, wherein said central processing unit is located in a server, and said memory is located in a client.